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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,535	04/08/2004	Mehmet Aslan	50019.0225USU1	8319

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EXAMINER	
VERBITSKY, GAIL KAPLAN	
ART UNIT	**PAPER NUMBER**
2855	
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10/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/820,535	ASLAN ET AL.	
	Examiner	Art Unit	
	Gail Verbitsky	~~2859~~ 2855	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *attachment #1*.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 6-11, 13-18, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida et al. (U.S. 6046492) [hereinafter Machida] in view Kunst.

Machida discloses in Fig. 23 a device comprising a temperature sensor having two (three) transistors/ junction diodes (collocated on the same substrate/ support) whose first electrode is connected to a first terminal A, a second electrode B is connected to a third terminal C (Vground/ Vbias), wherein only one of the first and second terminals A, B is connected to a measurement circuit 13 (and pad 14) by means of a switch 15. It is inherent, that the third terminal is used for temperature measurements (The numerals A-C have been added by the Examiner, see attachment # 1 to the Office Action).

Machida does not explicitly teach that the measurement circuit and the diode circuit are located on two separate substrates, and that the diode can have anode and cathode, as stated in claims 3, 10, 17, with the remaining limitations of claims 1-4, 6-11, 13-18, 20.

Kunst discloses in Fig. 6 a device in the field of applicant's endeavor and teaches that a measurement circuit including bias can be collocated on a single/ separate substrate 600. Kunst also teaches that diodes can be npn or pnp transistors or diodes, inherently, having anodes and cathodes (first and second electrodes respectively). For claims 7, 20: when measurements are

done by a first diode, two currents are applied to the first diode, as shown in Fig. 6. For claim 14: the temperature measurement circuit comprising an ADC.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device disclosed by the Machida, so as to replace transistors with diodes having anodes and cathodes, as taught by Kunst, because, as already suggested by Kunst, both of them, transistors and diodes, in this particular circuit, will perform the same function of producing temperature corresponding output junction measuring voltage.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device disclosed by Machida, so as to have the measuring circuit including diodes and bias circuit located on the same/ first substrate, as taught by Kunst, in order to obtain more accuracy of measurements by minimizing connecting lines to a remote bias location.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device disclosed by Machida, so as to have an ADC, as taught by Kunst, because, among other function, the ADC convert analog data to digital so as to make it transferable and readable from the computer.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device disclosed by Machida, so as to have couple different current directed to the same diode, in order to minimize the error by using difference in signals in time, as very well known in the art.

3. Claims 5, 12, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida and Kunst, as applied to claims 1-4, 6-11, 13-18, 20 above, and further in view of Prior Art by Sandhu et al. (U.S. 6140860) [hereinafter Prior Art].

Machida and Kunst disclose the device as stated above.

They do not explicitly teach that the bias circuit is formed on the second, third substrate or a discrete (separate) component, as stated in claims 5, 12, 19.

Prior Art teaches in Fig. 1 that a biasing circuit 10 can be located separately (separate discrete component) from a diode 14 (entire col. 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device disclosed by the Machida and Kunst, so as to have a measuring circuit with a biasing circuit separately of the substrate (and thus sensing diode) whose temperature being measured, as taught by Prior Art, so as to enable the operator to remotely obtain temperature measurements in the locations not easily accessible to the operator.

Response to Arguments

4. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection (new reference found).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art cited in the PTO-892 and not mentioned above disclose related devices and methods.

Kurihara (U.S. 5660474) discloses in Fig. 1 a device in the field of applicant's endeavor comprising two temperature measuring transistors 10 and 11, whose second electrodes (base) is

biased with a bias voltage by means of third terminals, first electrodes of transistors 10 and 11 are connected to first and second terminals respectively.

Lien (U.S. 6019508) discloses a device in the field of applicant's endeavor comprising first and second transistors 17-1 and 17-n.

Davidson et al (U.S. 5639163) discloses a device in the filed of applicant's endeavor wherein a temperature measuring circuit comprising biasing circuit (Vp), differential amplifier and ADC are located outside the first substrate/ chip.

Barton (U.S. 3181364) discloses in Fig. 1 a temperature sensing circuit comprising a dual diode system wherein first diode T1 has a first electrode (collector) and a second electrode (base) wherein the first electrode of T1 has the same polarity as a first electrode of a second diode T2, and the base of T1 has the same polarity as a base of T2. The device also has a first terminal through CRI is coupled to the first electrode of T1; a second terminal through CR2 is coupled to the first electrode of T2. A third terminals is coupled (biasing) by means of a bias circuit/ bias diode D1 the second electrodes (bases) of T1 and T2. The transistors are exposed to the same temperature. It is inherent, that the first polarity and the second polarity are different and opposite to each other. It is, inherent, that when voltage/ current is being measured, the third terminal must be used.

Grannes et al. (U.S. 7018095) discloses a device in the field of applicant's endeavor wherein a temperature measuring circuit is collocated on a second substrate and is configured to perform voltage measurements using at least first and second terminals.

Beer discloses a device in the field of applicant's endeavor wherein a temperature measuring circuit is collocated on a second substrate apart from a first substrate (entire col. 3).

Kunst (U.S. 6008685) Kunst discloses in Fig. 6 a device in the field of applicant's endeavor and teaches that a measurement circuit including bias can be collocated on a single/ separate (first) substrate 600. Kunst also teaches that diodes can be npn or pnp transistors (inherently, having emitters) or diodes, inherently, having anodes and cathodes (first and second electrodes respectively. Kunst also teaches a first terminal connected to a first electrode (cathode) of a diode 650-1, a second terminal connected to a first electrode (cathode) of a second diode 650-2, and a third electrode/ bias circuit) biasing (grounding) second (anodes) electrodes of the diodes.

Shih (U.S. 20030133491 filing date 01/04/2002) Shih discloses in Fig. 1 a device in the field of applicant's endeavor comprising a dual diode system (D1, D2). In calibration mode, Shih teaches to provide a first current through both diodes, while, in the run (operation) mode, Shih teaches to provide a second current only to the first diode, inherently using, only first terminal for two currents.

Miranda, Jr. et al. (U.S. 6097239) [hereinafter Miranda]

discloses in Fig. 1 a device in the field of applicant's endeavor having a first diode (transistor) 16 and a second (reference) diode (transistor 20. Miranda teaches to obtain junction voltage of the diode 16 by using two different currents 26 and 28 for compounding a single Vbe (col. 6, line 8). Miranda states that both diodes/ junctions can be located on the same (first) chip/ substrate (col. 5, lines 4-10). The device has a first terminal (connected to the first electrode/ emitter 35 of the junction 16, a second terminal connected (connected to the second electrode/emitter at 22 of the junction 200 and a third terminal (ground) is connected to the second electrodes (collectors) of the junctions 16 and 20. Miranda states that the transistors can be of any polarity combination (col. 5, lines 14-20), thus, satisfying the limitations of claim 1.

The first and second junction diodes are, inherently have bases.7

Tuthill (U.S. 5982221) discloses in Fig. 3 a device in the field of applicant's endeavor comprising a dual diode temperature sensor (transistors 66 and 68) collocated on a common substrate wherein emitters (first electrodes) of the transistors are connected to first terminal C1 and second terminal C2 respectively, bases (second electrodes) are biased with AGND (biasing circuit) by means of a third terminal, wherein the first electrodes have polarity opposite to the second electrodes. The device further comprises a differential ADC part of which is a differential amplifier 78. All the terminals are used to measure temperature-related voltage. It is inherent, that that the terminals are coupled to the electrodes by means of couplings/ connections, as shown in Fig. 3.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gail Verbitsky whose telephone number is 571/ 272-2253. The examiner can normally be reached on 7:30 to 4:00 ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on 571/ 272-2245. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GKV

Gail Verbitsky
Primary Patent Examiner, TC 2800

October 05, 2007

FIG. 21

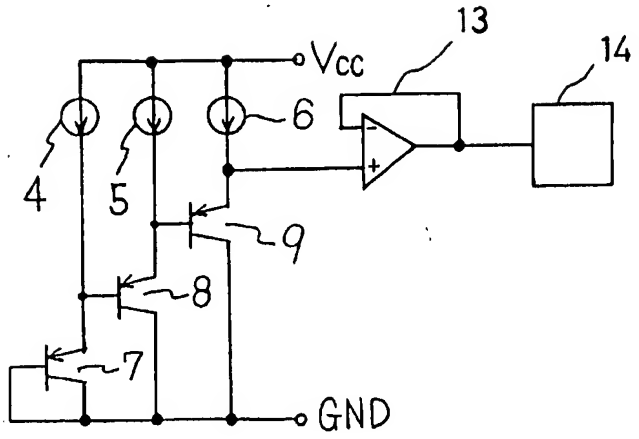
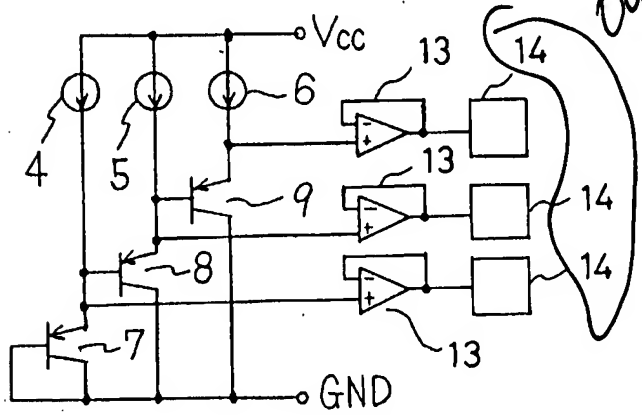
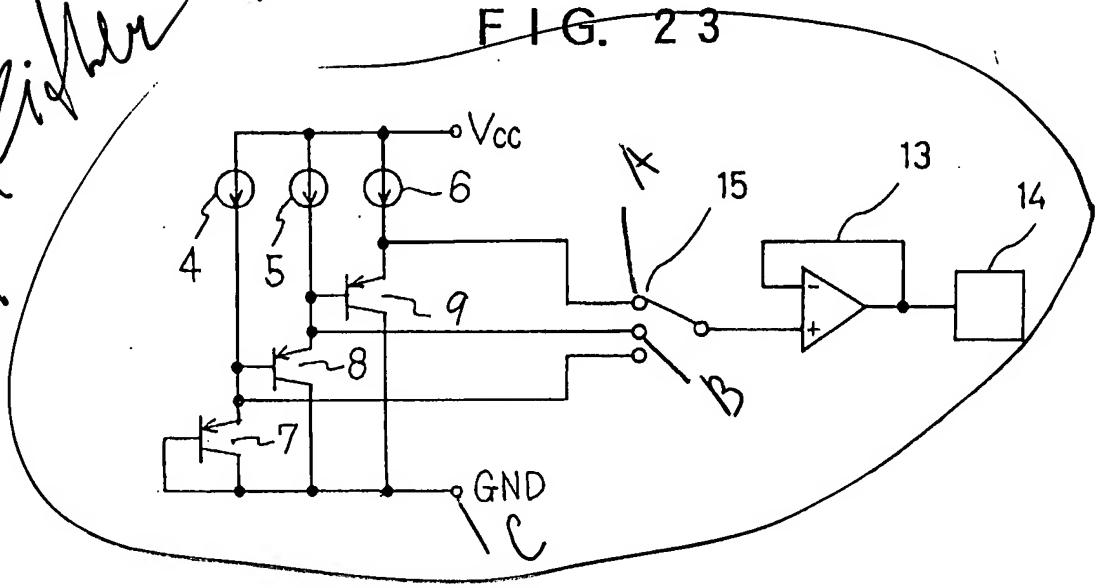


FIG. 22



output pads

FIG. 23



attachment #1
(10820535)